Please amend the application as follows:

In the Specification:

In the paragraph on pages 3, 4 and 5:

FIG. 1 illustrates an embedded memory system 10 having error correction circuitry with a counter for counting detected errors during normal read and write cycle operation. An MRAM core 12 is generally illustrated. It should be understood that the MRAM core 12 contains column and row decoders, read sense amplifiers and write drivers that are not specifically illustrated. The MRAM is accessed by an address bus that receives an address value labeled "Address". The MRAM core 12 also has an error, read and write counts field 14 that is a special memory location for storing error counts, read cycle counts and write cycle counts. An input buffer 16 has an input coupled to a bus for receiving input data labeled "Data In". An output of the input buffer 16 is connected via a bus to an input of an Error Correction Code (ECC) coder 18. An output of the ECC coder 18 is connected to a data input of the MRAM core 12 via a bus. A data output of the MRAM core 12 is connected via a bus to an input terminal of an ECC corrector 20. A first output of the ECC corrector 20 is connected to an input of an output buffer 22. An output of the output buffer 22 provides output data labeled "Data Out". An error counter 24 has an input connected to a second output of the ECC corrector 20 via a bus. An output of the error counter 24 is connected to a second input of the ECC coder 18 via a bus. The second output of the ECC corrector 20 is also connected to an input of a write cycle counter 26. An output of the write cycle counter 26 is connected to the second input of the ECC coder 18 via the bus that the output of error counter 24 is connected to.

The second output of the ECC corrector 20 is also connected to an input of a read cycle counter 28. The output of the read cycle counter 28 is connected to the second input of the ECC coder 18 via the bus that the output of error counter 24 is connected to. A control circuit 30 has a first input for receiving a Read control signal and a second input for receiving a Write control signal. A first output of control circuit 30 is connected to a control terminal of the MRAM core 12. A second output of ~~the MRAM core 12~~ control circuit 30 is connected to a control input of the ECC coder 18. A third output of the control circuit 30 is connected to a control input of the ECC corrector 20. A fourth output of the control circuit 30 is connected to a control input of the output buffer 22. A fifth output of the control circuit 30 is connected to a control input of the error counter 24. A sixth output of the control circuit 30 is connected to a control input of the write cycle counter 26. A seventh output of the control circuit 30 is connected to a control input of the read cycle counter 28. An eighth output of the control circuit 30 is connected to a second input of the read cycle counter 28 for providing a Read Pulse signal. A ninth output of the control circuit 30 is connected to a second input of the write cycle counter 26 for providing a Write Pulse signal. A tenth output of the control circuit 30 is connected to a second input of the input buffer 16 for controlling storage timing of input buffer 16. A third output of the ECC corrector 20 is connected to a third input of the error counter 24 and to a third input of the control circuit 30.